Amendments to the Claims

This listing of claims will replace all prior versions, and listing, of claims in the application.

1. (Previously presented) A thin film diode array panel comprising:

an insulating substrate;

first and second redundant gate lines made of an opaque conductor and formed on the insulating substrate;

first and second floating electrodes made of an opaque conductor, formed on the insulating substrate, and disposed between the first and second redundant gate lines;

an insulating layer formed on the first and second floating electrodes;

a first gate line formed at least partially directly on the first redundant gate line and including a first input electrode overlapping the first floating electrode wherein the insulating layer is interposed between the first input electrode and the first floating electrode, and further wherein the insulating layer entirely covers lateral surfaces of the first floating electrode;

a second gate line formed at least partially directly on the second redundant gate line and including a second input electrode overlapping the second floating electrode [[where]] wherein the insulating layer is interposed between the second input electrode and the second floating electrode and further wherein the insulating layer entirely covers lateral surfaces of the second floating electrode; and

a pixel electrode including a first contact electrode overlapping the first floating electrode where the insulating layer is interposed between the first contact electrode and the first floating electrode, a second contact electrode overlapping the second floating electrode where the insulating layer is interposed between the second contact electrode and the second floating electrode, and a main body.

2. (Original) The thin film diode array panel of claim 1, wherein the first and second redundant gate lines and the first and second floating electrodes are made of Mo, and the pixel electrode and the first and second gate lines are made of indium tin oxide (ITO).

3. (Original) The thin film diode array panel of claim 1, wherein the insulating layer includes a first insulating layer regionally formed around the first floating electrode, and a second insulating layer regionally formed around the second floating electrode.

4. (Original) The thin film diode array panel of claim 1, wherein the insulating layer covers the first and second redundant gate lines and the first and second floating electrodes and has contact holes exposing the first and second redundant gate lines, and the first and second gate lines are connected to the first and second redundant gate lines through the contact holes.

5. (Original) The thin film diode array panel of claim 1, wherein the insulating layer covers the first and second redundant gate lines and the first and second floating electrodes and has cutout stripes exposing the first and second redundant gate lines, and the first and second gate lines are connected to the first and second redundant gate lines through the cutout stripes.

6. (Original) The thin film diode array panel of claim 4, wherein the insulating layer has a cutout disposed to overlap at least a portion of the main body of the pixel electrode.

7. (Original) The thin film diode array panel of claim 6, wherein the cutout is disposed under the main body of the pixel electrode and exposes a portion of the insulating substrate around the main body of the pixel electrode.

8. (Previously Presented) A thin film diode array panel comprising:

an insulating substrate;

first redundant gate lines including a first input electrode and made of an opaque conductor;

second redundant gate lines including a second input electrode and made of an opaque conductor;

first and second contact electrodes formed on the insulating substrate and made of an opaque conductor;

an insulating layer formed on the first and second input electrodes and the first and second contact electrodes;

a first gate line formed at least partially directly on the first redundant gate line;

a second gate line formed at least partially directly on the second redundant gate line;

a first floating electrode formed on the insulating layer and overlapping the first input electrode and the first contact electrode;

a second floating electrode formed on the insulating layer and overlapping the second input electrode and the second contact electrode; and

a pixel electrode connected to the first and second contact electrodes.

9. (Original) The thin film diode array panel of claim 8, wherein the first and second redundant gate lines and the first and second contact electrodes are made of Mo, and the pixel electrode and the first and second gate lines are made of indium tin oxide (ITO).

10. (Original) The thin film diode array panel of claim 8, wherein the insulating layer includes a first insulating layer regionally formed around the first floating electrode and a second insulating layer regionally formed around the second floating electrode.

11. (Original) The thin film diode array panel of claim 8, wherein the insulating layer covers the first and second redundant gate lines and the first and second contact electrodes and has contact holes exposing the first and second redundant gate lines, and the first and second gate lines are connected to the first and second redundant gate lines through the contact holes.

12. (Original) The thin film diode array panel of claim 8, wherein the insulating layer covers the first and second redundant gate lines and the first and second contact electrodes and has cutout stripes exposing the first and second redundant gate lines, and the first and second gate lines are connected to the first and second redundant gate lines through the cutout stripes.

13. (Original) The thin film diode array panel of claim 11, wherein the insulating layer has a cutout disposed to overlap at least a portion of the main body of the pixel electrode.

14. (Original) The thin film diode array panel of claim 13, wherein the cutout is disposed under the main body of the pixel electrode and exposes a portion of the insulating substrate around the main body of the pixel electrode.